AN10439

Wafer Level Chip Size Package

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Document information

Info	Content
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Abstract	This application note provides guidelines for the use of Wafer Level Chip Size Packages (WLCSP). For information on printed circuit board (PCB), footprint design and reflow soldering see application note *AN10365 (Surface mount reflow soldering description*).

Revision history

Rev	Date	Description
03	20071017	Third version (external release); adapted to NXP house style
02	20060713	Second version (internal release); minor changes
01	20060310	First version (internal release)

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1. Introduction

This application note provides the guidelines for the use of Wafer Level Chip Size Packages (WLCSP). Useful general information on the subject of printed circuit board (PCB), footprint design and the reflow soldering processes will be provided by reference to application note *AN10365 (Surface mount reflow soldering description)*. It is strongly recommended to read AN10365 prior to, or in conjunction with, this one. This note also provides special clarification which applies to the general rules regarding WLCSP.

The information in this application note can be used throughout the various stages of WLCSP use. First, a more detailed description is provided of the product and the way it is delivered. Then recommendations for Printed Circuit Board (PCB) layout can be found. These should be used during the end product development phase. The guidelines for assembly and manual rework and handling can be helpful in the production flow. The document concludes with a chapter about the reliability qualification of WLCSPs.

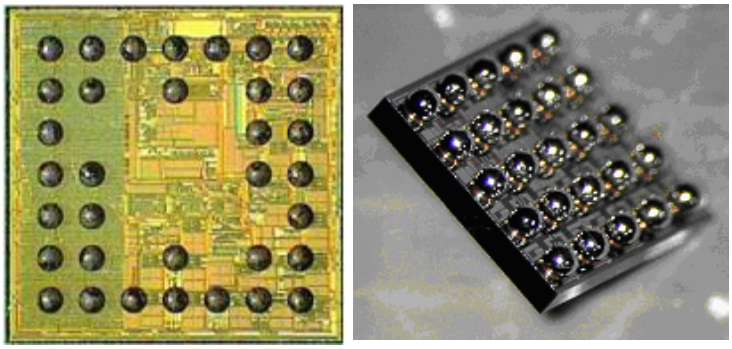

Fig 1. WLCSP Radio IC and 10 channel filter viewed at the bump side

2. Product description

A WLCSP is a package that is the same size as the bare die. This is the most effective way of achieving higher circuit densities and miniaturization.

The interconnection from the die to the PCB is achieved by solder bumps also called solder balls applied onto the wafer. The main advantage of WLCSP packaging technology is that the IC to PCB inductance is minimized because there are no leads, bond wires or interposer connections. Furthermore package size, cost and thermal characteristics are optimized. For a significant portion of shipped WLCSP products the solder ball footprint now determines the size. A reduction of the solder ball pitch automatically results in reduced die size and therefore also cost. Due to the permanent price pressure a clear trend towards smaller pitches is visible.

The WLCSP is packaged on wafer level, which means the ICs are all on the wafer during the back end processing which include applications like passivation, bumping and testing. After separation of the dies, they are ready for mounting. The most common packing method for WLCSP is tape and reel. In this packing the components are ready to be used in pick and place equipment. For more information, see Section 3.

The bumping process consists of the formation of an under bump metallization (UBM) which connects the alumina pad of the die to the solder ball and the placement of solder balls. If required, a passivation layer can be placed before the bumping process. The passivation layer provides mechanical stress relief for the solder bumps as well as electrical and environmental isolation at the die surface.

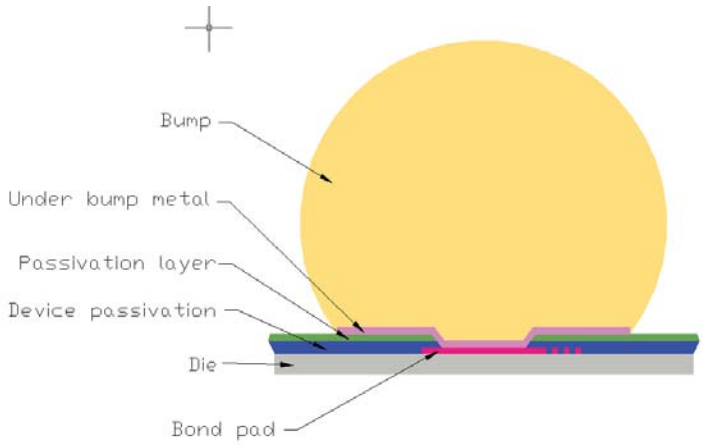

Fig 2. Bump design

A WLCSP is attached to the PCB facedown. The interconnection is from the die pad via the bump to the PCB pad. Because the solder balls are relative large, the chip size package can be mounted on a PCB without under filling and this keeps the assembly process simple.

Fig 3. Identity plate

A photograph of the top side of a WLCSP package, in this case a FM Radio IC, is shown in Figure 3.

3. Tape and reel

The WLCSP products are placed into tape and reel with every die being placed into a separate pocket. This is carried out with the soldered bumps on the WLCSP facing downwards. In this way, the pick and place equipment on the PCB assembly line can pick the packages out of the pockets and place them directly onto the PCB.

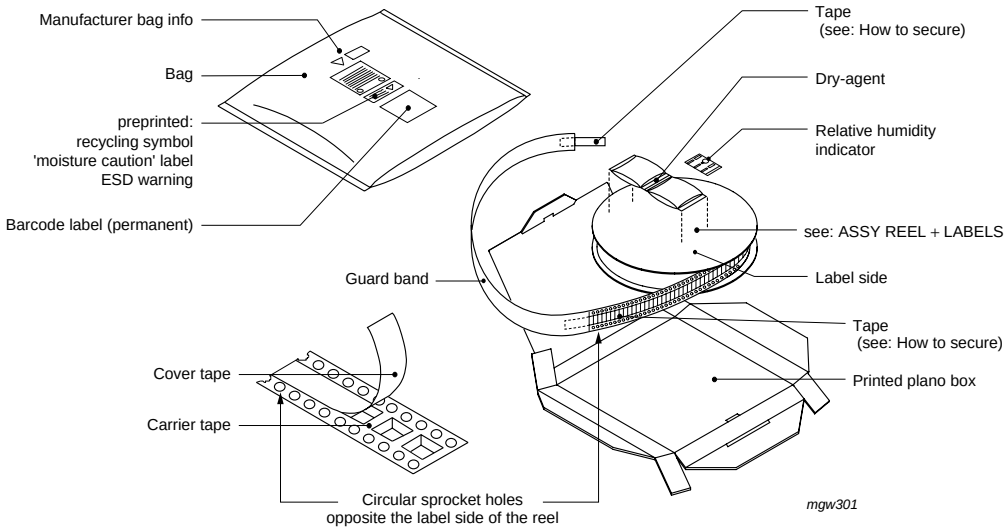

Fig 4. Tape and reel overview

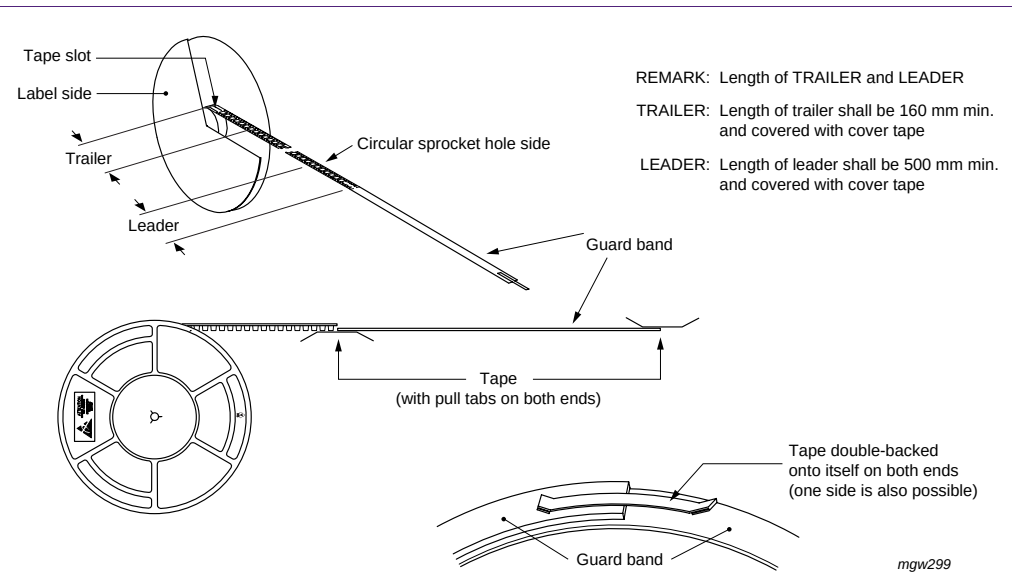

Fig 5. Tape and reel design

The qualification of the packing method is part of the release of the product. This qualification is carried out by the NXP packing organization. An overview of the tests performed for new or modified packing material is shown below.

- Visual check
- Dimensions (ANSI/EIA-481-C)
- Operation
- Surface conductivity according to EIA541
- Tensile strength according to IEC60286
- Elongation
- Peel-off strength according to EIA481/IEC60286
- Drop test according to UN-D1400
- Material content (environmental requirements)
- Vibration test according to UN-D1400 (optional)

4. Board design recommendations

Creating the proper PCB design will ensure a trouble free start when using WLCSP. This does not only concern the footprint design but also the location of the WLCSP product on the board.

4.1 Footprint layout

Figure 6 shows the 2 types of recommended WLCSP solder pads, solder mask defined (SMD) pads and copper (Cu) defined pads, also known as non solder mask defined (NSMD) pads. There is no preference between solder resist or Cu defined pads. A solder pad of 280 μm in diameter is required for a 0.5 mm pitch device. For a 0.4 mm pitch device this is 235 μm. To get the best controlled pad definition please contact your board supplier.

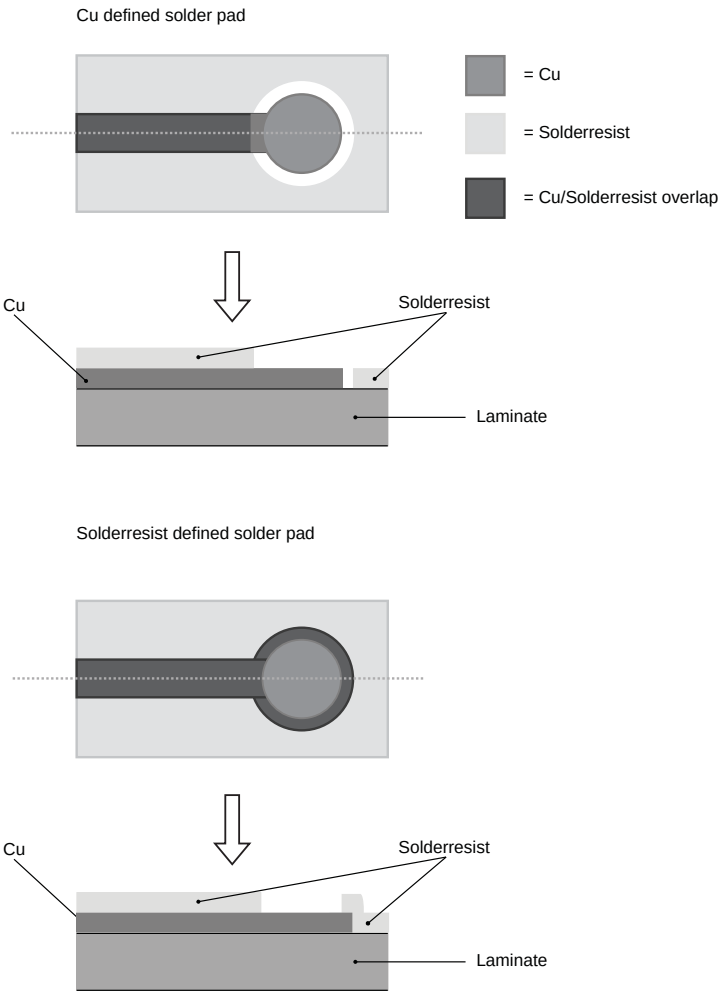

Fig 6. Recommended WLCSP solder pads

It is recommended that the whole internal area of the pad be flat. This means that the use of via's under the bumps should be avoided wherever possible as non-flat surfaces can create voids in the solder joint and reduce the reliability.

The connection of single pads directly to large areas of solid metal (e.g. ground planes), should be avoided as this can result in cold spots on certain balls. During cool down, these cold solder balls will already solidify while the surrounding balls are still melted. This will apply stress to the integrated circuit. It is better to have a balanced amount of metal to all pads so that all balls solidify at the same time.

4.2 Clearances

For a typical advanced electronic equipment board, clearance around the maximum size of the component should be taken into account. This is to accommodate for the pick and placement accuracy of the WLCSP component as well that of the surrounding components.

Just like for all other surface mounted components, the placing of WLCSP products near mounting holes, connectors, clamps etc. is not recommended. This is due to the increased amount of bending stress on the bumps and/or the chance of hitting the product during assembly or during use of the end product.

Usually during PCB assembly multiple PCBs are part of a larger panel. The separation of this panel in single PCBs can result in mechanical stress to components that are mounted near the separation lanes. A certain amount of clearance from the separation lane should be advised by the factory. This clearance depends on the separation process.

5. Assembly process

The application note AN10365 describes the surface mounting assembly process. WLCSPs are mounted in exactly the same way as all other types of surface mount components. Because the WLCSP is not protected by a plastic package, some additional directions for use are given in this application note.

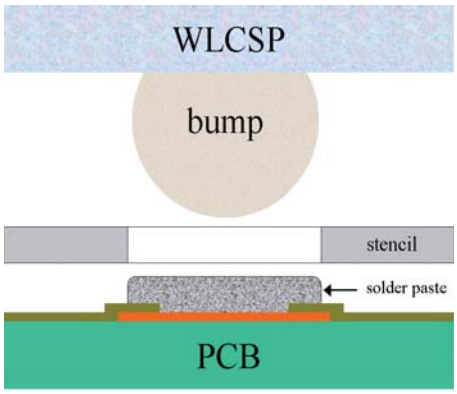

Fig 7. Stencil printing and WLCSP placement

The WLCSP mounting process of placing the bumps in stencil printed solder paste is the most robust method. Stencil thicknesses of between 100 μm and 150 μm are common for packages of this kind. The stencil aperture is chosen such that the maximum amount of solder is applied. This ensures a maximum bump height and therefore maximum board level reliability. The dimensions of a typical aperture are between the same size as the underlying pad and up to 50 μm smaller.

Larger apertures can cause yield loss due to solder shorts. The tapes in which the WLCSP products are transported should be handled with care. They should not be dropped on the ground, nor bent at extreme angles.

WLCSP placement is carried out in the same way as other surface mounted components. The alignment of the component should be carried out using a camera system because mechanical clamps or other mechanical alignment methods can cause damage to the product.

When compared to HVQFN packages, WLCSPs are more vulnerable when touching neighboring components. It should therefore be made clear that the WLCSP should be transported high enough above the PCB before the downward placing motion starts. In general the clearance in both the vertical and horizontal directions should be equal. See Figure 8.

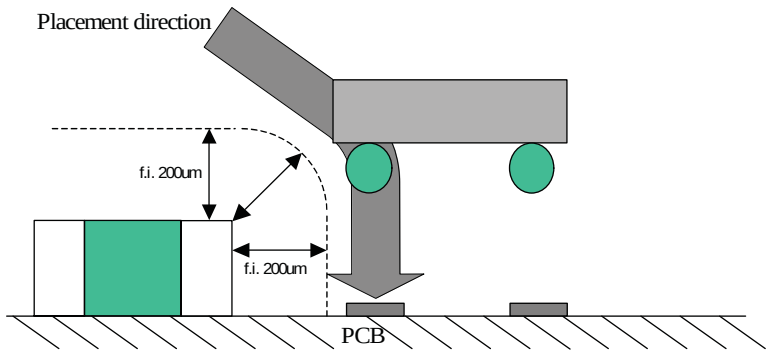

Fig 8. Component clearances

Even though a layer of printed solder paste can absorb some of the force, in order to reduce the impact during placement to a minimum, it is recommended that WLCSPs are placed coplanar to the PCB surface.

The use of a larger type of nozzle is preferred. From a mechanical point of view, there are no special requirements with respect to nozzle material. A dissipative nozzle material will prevent static electricity from building up. Except for the clear advantages in ESD prevention, this will also ease the release of the component from the nozzle. Most pick and place equipment have arrangements that cause the nozzles to slow down when approaching the PCB surface in order to keep the placement impact force minimal. These arrangements should be enabled during WLCSP placement.

6. Rework process and manual handling

In cases when a replacement part is required it is advised that a BGA rework station be employed. See Figure 9.

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable.

Removal, will cause damage to the solder balls and therefore a removed sample cannot be reused.

Please take notice of chapter 'Inspection and repair' in application note AN10365 to find more information on board cleaning and site preparation.

Fig 9. Rework station

7. Reliability

NXP has done extensive testing of WLCSP packages to provide the optimum manufacturing conditions for assembly and to assure the necessary proof of long term reliability in consumer equipment. This enables customers to use the package with high confidence.

The tests shown below are performed to prove that NXP WLCSP technology is robust and reliable. For example corrosion, UBM adhesion and solder fatigue are failure mechanisms that have been investigated thoroughly.
Reliability testing during technology development has resulted in optimum settings and design rules for the WLCSP and its board assembly.

During qualification reliability tests are performed on wafer level, products and on board level resulting in optimal quality level under all circumstances.

Overview of reliability tests and results for typical WLCSP package/products:

Table 1. Reliability tests

Test	Conditions	Criteria	Results
Ball shear	0 h	ball shear force	passed
Multiple reflow	Pb-free reflow profile, 1..10x	ball shear force	passed
Moisture resistance	MSL1	JEDEC MSL1	passed
TMCL	–55/+125 °C, 500/1000 cycles	3x 0/77	passed
		3x < 0.2 % fails/wafer	passed
UHST	130 °C, 85 % RH, 96/192 h	3x 0/77 functional	passed
		ball shear force 3x 0/50, no corrosion	passed
HTSL	150 °C, 1008 h	3x < 0.2 % fails/wafer ball shear force (UBM adhesion to passivation/ metal pad)	passed
THB	85 °C, 85 % RH, 1008 h	3x 0/32	passed

Board level reliability tests:

Table 2. Board level reliability tests

Test	Conditions	Criteria	Results
TMCL	–40/+125 °C, 300 cycles	3x 0/77, solder fatigue	passed
UHST	130 °C, 85 % RH, 96/192 h	3x 0/77	passed
Drop test	1500 G, 0.5 ms, half sine	JEDEC, 30 drops	passed

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